

II B.Tech II Semester Regular Examinations, Apr/May 2008
LINEAR AND DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering and Instrumentation &
Control Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Derive closed loop voltage gain, input resistance, output resistance and bandwidth for inverting amplifier with feedback arrangement. [10+6]
(b) Explain any one of the frequency compensation technique in connection with Op-amp.
2. (a) Explain how Op-amp used as a integrator and differentiator.
(b) With the help of a neat circuit diagram, explain the operation of instrumentation amplifier of obtain the expression for its o/p voltage V_O . [8+8]
3. (a) Define a Notch filter. Give its application.
(b) Determine the order of the Butterworth low-pass filter so that at $\omega = 1.5\omega_{3dB}$, the magnitude response is down by at least 30 dB.
(c) Design a notch filter for $f_o = 8$ kHz and quality factor $Q=10$. Choose $C=500$ pf and assume necessary data. [5+6+5]
4. (a) Describe the operation of an analog phase detector.
(b) Analyze the behavior of an analog phase detector through necessary circuit diagram, waveforms, mathematical expressions and characteristic curves.[8+8]
5. (a) Sketch and explain the transfer characteristic of a DAC with necessary equations.
(b) LSB of a 9-bit DAC is represented by 19.6 m Volts. If an input of 9 zero bits is represented by 0 volts.
 - i. Find the output of the DAC for an input, 10110 1101 and 01101 1011.
 - ii. What is the Full scale Reading (FSR) of this DAC? [8+8]
6. (a) Draw the schematic circuits of CMOS NAND and CMOS NOR gates and explain their functions with the help of Truth-Table.
(b) What are the advantages and disadvantages of CMOS over TTL gate?
(c) Which is the fastest saturated logic gate? and Why? [8+4+4]
7. (a) Write short notes on n- Bit parallel adder.
(b) Design a driver circuit for LCD display. [8+8]
8. (a) Explain with an example why asynchronous inputs are required in flip flops.

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(b) Explain the operation of edge triggered T flip- flop.

[8+8]

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1. (a) What is cross over distortions and how it is eliminated in differential amplifier?
(b) Explain different methods of external frequency compensation in an Op-amp.
(c) Design an amplifier with a gain of +5 using one Op-amp (make necessary assumptions). [4+6+6]
2. (a) What is a clipper? With circuit diagram, explain the operation of positive and negative clippers.
(b) Describe the principle of operation of a precision half wave rectifier with wave forms. [10+6]
3. (a) Derive the expression for frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit.
(b) Design a second order low pass filter at a high cut off frequency of 1 KHz. Derive the transfer function of the above filter. [8+8]
4. (a) Draw and explain the functional diagram of a 555 Timer.
(b) Explain the function of 'reset' pin. [14+2]
5. (a) Sketch and explain the transfer characteristic of a DAC with necessary equations.
(b) LSB of a 9-bit DAC is represented by 19.6 m Volts. If an input of 9 zero bits is represented by 0 volts.
 - i. Find the output of the DAC for an input, 10110 1101 and 01101 1011.
 - ii. What is the Full scale Reading (FSR) of this DAC? [8+8]
6. List out advantages, disadvantages & applications of MOS logic. [16]
7. (a) Design 1:8 Demultiplexer using two 1:4 Demultiplexer?
(b) Realize the following expression using 74×151 ICs and 74×139 IC [8+8]
$$F(Z) = ABCD + \overline{A}\overline{B}CD + AB\overline{C}D + ABDE + AC\overline{D}\overline{E} + \overline{A}\overline{B}CE + ABC\overline{D}$$
8. (a) Distinguish between Combinational circuits and sequential circuits.
(b) Write short notes on Clocked SR flip flop. [8+8]

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1. (a) List out the ideal characteristics of an Op-amp.
 (b) With neat block diagram explain the function of various building blocks of an Op-amp.
 (c) Draw the equivalent circuit of an Op-amp. [3+10+3]
2. (a) Explain the operation of Zero crossing detector.
 (b) Briefly mention the disadvantages of using Zero crossing detector and how it is overcome in Schmitt Trigger?
 (c) Draw a circuit using Op-amp which can work as adder (inverted and non-inverted) and explain how it works. [4+4+8]
3. (a) Design a II order Butterworth Low-pass filter for a cut off frequency of 1KHz and for a given normalized polynomial of $S^2+1.414S+1$. Assume necessary data.
 (b) In the above circuit given (figure 3(b)ii) if the integrator components are $R_1=120\text{ K}\Omega$ and $C_1 = 0.01\mu\text{F}$, $R_3= 6.8\text{ K}\Omega$ $R_2= 1.2\text{K}\Omega$, determine
 - i. Peak-to-peak triangular output amplitude.
 - ii. The frequency of triangular wave. [8+8]

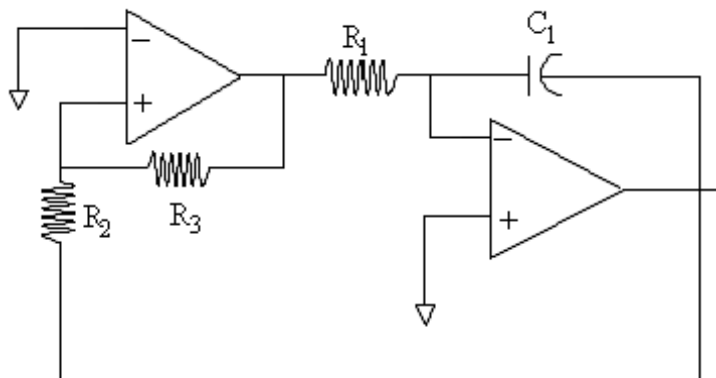


Figure 3(b)ii

4. (a) Design a 555 Astable multivibrator to operate at 10 KHz with 40% duty cycle.
 (b) Explain in which the 555 timer can be used as Astable multivibrator. [8+8]
5. (a) Draw the block diagram for a 2-bit parallel-comparator A/D converter and explain the operation of the system.

- (b) Draw a schematic diagram of a ladder network D/A converter. Explain the operation of the converter. [8+8]
- 6. (a) Explain the operation of open drain output of CMOS?
(b) Explain the behavioral difference between simple transistor logic inverter and Schottky logic inverter? [8+8]
- 7. (a) What is multiplexer? Draw the logic diagram of 4 to 1 line multiplexer?
(b) Design half adder using NAND gates only? [8+8]
- 8. (a) Explain with the help of neat diagram the simple structure of MOS ROM.
(b) Design MOD 5 synchronous counter. [8+8]

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1. (a) Give the pin diagram of IC741 and give its specifications.
(b) Discuss the differences between the differential amplifiers used in the first two stages of Op-amp. [8+8]
2. (a) Explain the operation of Zero crossing detector.
(b) Briefly mention the disadvantages of using Zero crossing detector and how it is overcome in Schmitt Trigger?
(c) Draw a circuit using Op-amp which can work as adder (inverted and non-inverted) and explain how it works. [4+4+8]
3. (a) The cutoff frequency of a certain first order low pass filter is 2 KHz. Convert this low pass filter to have a cutoff frequency of 3 KHz by using the frequency scaling technique.
(b) How do we get a Notch filter from a band pass filter.
(c) What are the advantages of active filters over passive filters. [8+4+4]
4. (a) Give the block diagram of PLL and explain about each block in detail.
(b) Define the following terms with reference to PLL.
 - i. Lock range.
 - ii. Capture range.
 - iii. Pull-in-time. [10+6]
5. (a) Draw and compare the conversion times for tracking and successive approximation ADC devices.
(b) A dual slope ADC uses a 12bit counter and a 8 MHz clock rate. The max input voltage is +10V. The maximum integrator o/p voltage should be -8V, when the counter has cycled through 2^n counts. The capacitor used in the integrator is $0.1\mu\text{F}$. Find the value of the resistor of the integrator. [8+8]
6. (a) Explain the following terms with reference to TTL gate?
 - i. Logic levels.
 - ii. DC Noise margin.
 - iii. Low-state unit load.
 - iv. High-state fan out.

- (b) List out TTL families and compare them with reference to propagation delay, power consumption, speed-power product and low level input current? [8+8]
- 7. (a) Design the combinational circuit for common cathode 7 segment display/driver?
(b) Write short notes on gray code to Binary converter. [8+8]
- 8. (a) Write a note on applications, advantages and disadvantages of SRAM.
(b) Design MOD 6 synchronous counter. [8+8]

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