

II B.Tech II Semester Regular Examinations, Apr/May 2008
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. Convert the following to Decimal and then to Octal.

(a) 1234_{16}

(b) $12EF_{16}$

(c) 10110011_2

(d) 10001111_2

(e) 352_{10}

(f) 999_{10}

[3+3+3+3+2+2]

2. (a) Simplify the following Boolean expressions to minimum no. of literals. [8]

i. $ABC + A'B + ABC'$

ii. $(BC' + A'D)(AB' + CD')$

iii. $x'yz + xz$

iv. $xy + x(wz + wz')$

(b) Obtain the Dual of the following Boolean expressions. [8]

i. $AB + A(B + C) + B'(B + D)$

ii. $A + B + A'B'C$

iii. $A'B + A'BC' + A'BCD + A'BC'D'E$

iv. $ABEF + ABE'F' + A'B'EF$

3. (a) Reduce the following function using K-map and implement it in AOI logic as well as NOR logic $F = \prod M(0, 1, 2, 3, 4, 7)$ [10]

(b) What do you mean by K-map? Name its advantages and disadvantages [6]

4. Explain the type of Hazard if any in the EXCLUSIVE - OR circuit made by five NAND gates and the EXCLUSIVE ?OR circuit made by four NAND gates as shown in figure 4. [16]

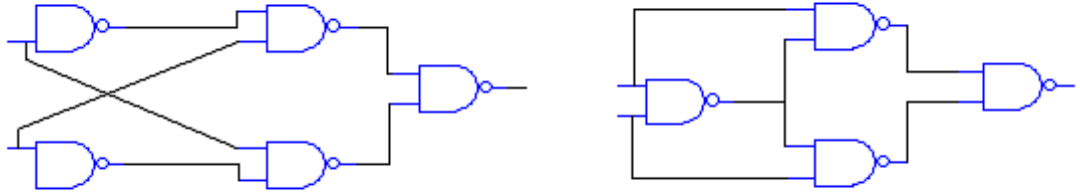


Figure 4

5. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.
 (b) For the given 3-input, 4-output truth table of a combinations circuit, tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

6. (a) Compare synchronous & Asynchronous circuits
 (b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]
7. (a) Determine the equivalence classes for the given state - table.
 (b) Obtain final transition table. [8+8]

Present state q^v	Next state q^{v+1}, x^2				Output z^v			
	x=0	x=1	x=2	x=3	x=0	x=1	x=2	x=3
q_0	q_4	q_2	q_1	q_4	1	0	1	1
q_1	q_2	q_5	q_4	q_1	0	1	1	0
q_2	q_1	q_0	q_3	q_5	1	0	1	1
q_3	q_6	q_5	q_4	q_1	0	1	1	0
q_4	q_2	q_5	q_3	q_4	0	1	1	0
q_5	q_2	q_5	q_3	q_7	1	1	0	0
q_6	q_3	q_0	q_1	q_5	1	0	1	1
q_7	q_1	q_2	q_4	q_5	1	0	1	1

8. (a) For the given ASM chart obtain its equivalent state diagram 8.
 (b) Design the circuit using multiplexes. [8+8]

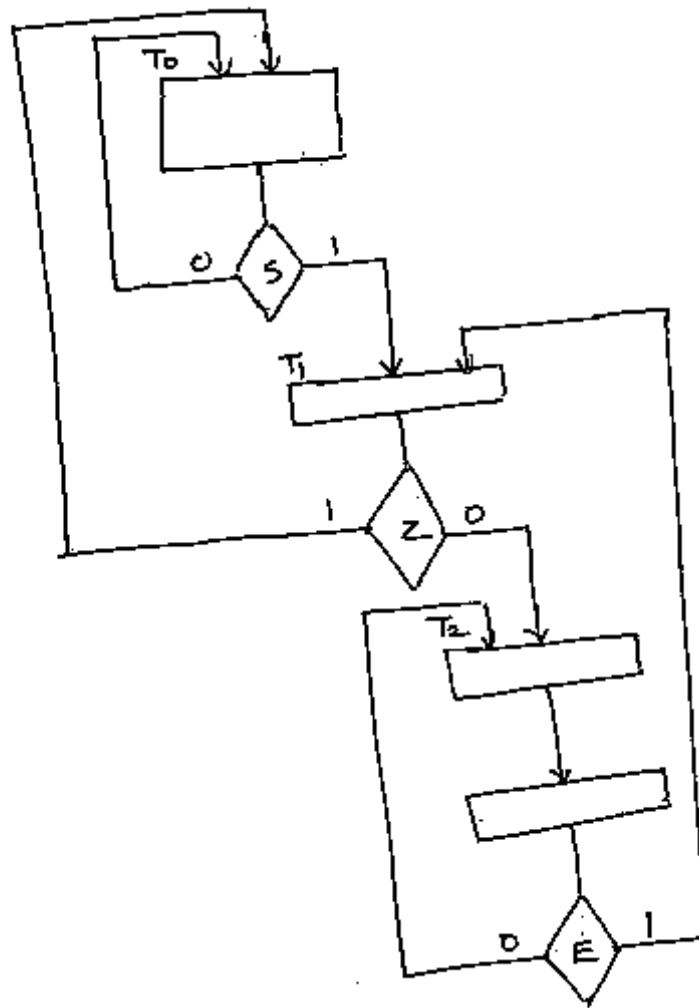


Figure 8

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1. Convert the following to Decimal and then to Binary.

(a) 1011_{16}

(b) $ABCD_{16}$

(c) 7234_8

(d) 7766_8

(e) 128_{10}

(f) 720_{10} .

[3+3+3+3+2+2]

2. (a) Express the following functions in sum of minterms and product of maxterms. [8]

i. $(xy+z)(y+xz)$

ii. $B'D+A'D+BD$

(b) Obtain the complement of the following Boolean expressions. [8]

i. $AB'C+AB'D+A'B'$

ii. $A'B'C+ABC'+A'B'C'D$

iii. $ABCD+ABC'D'+A'B'CD$

iv. $AB+ABC'$

3. (a) For the truth table given below , find the minimal expression for the out put (Y) using K-map [8+8]

Inputs				Output(Y)
A	B	C	D	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

(b) Expand $A + B\bar{C} + AB\bar{D} + ABCD$ to minterms and maxterms.

4. (a) Design a combinational logic to subtract one bit from the other. Draw the logic diagram using NAND and NOR gates.

(b) Explain the working of a serial adder. [12+4]

5. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

(b) For the given 3-input, 4-output truth table of a combinations circuit, tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

6. (a) Compare synchronous & Asynchronous circuits

(b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output $Z = 1$ and overlapping is also allowed.

- (a) Obtain State - Diagram.
 (b) Also obtain state - Table.
 (c) Find equivalence classes using partition method & design the circuit using D - flip-flops. [4+4+8]

8. For the ASM chart given 8:

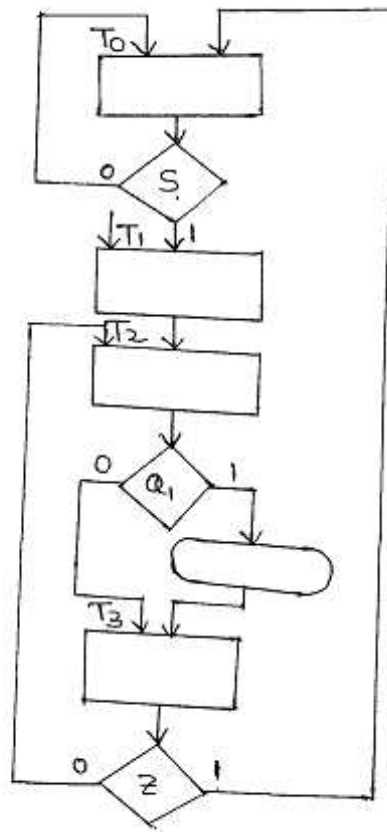


Figure 8

- (a) Draw the state diagram.
 (b) Design the control unit using D flip-flops and a decoder. [8+8]

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1. Convert the following to Decimal and then to Binary.
 - (a) 2311_{16}
 - (b) $A44D_{16}$
 - (c) 7444_8
 - (d) 7667_8
 - (e) 158_{10}
 - (f) 729_{10} [3+3+3+3+2+2]
2. (a) Simplify the following Boolean expressions. [8]
 - i. $A'C' + ABC + AC'$ to three literals
 - ii. $(x'y' + z)' + z + xy + wz$ to three literals
 - iii. $A'B(D' + C'D) + B(A + A'CD)$ to one literal
 - iv. $(A' + C)(A' + C')(A + B + C'D)$ to four literals
- (b) Obtain the complement of the following Boolean expressions. [8]
 - i. $B'C'D + (B + C + D)' + B'C'D'E$
 - ii. $AB + (AC)' + (AB + C)$
 - iii. $A'B'C' + A'BC' + AB'C' + ABC'$
 - iv. $AB + (AC)' + AB'C$
3. (a) What is a cell of a K-map? What is meant by pair, a quad, and an octet of a map and how many variables are eliminated? [8]
- (b) Reduce the following function using K- map and implement it using NAND logic. $F = \sum m(0, 2, 3, 4, 5, 6,)$ [8]
4. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.

$$Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D}$$

$$Y_2 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}$$

$$Y_3 = \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BC\bar{D}$$
- (b) Explain the terms Multiplexing and Demultiplexing. [10+6]
5. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

- (b) For the given 3-input, 4-output truth table of a combinations circuit, tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

6. (a) Design a sequence detector which detects 110010. Implement the sequence detector by using D - type flipflops.
- (b) Classify the required circuits into synchronous, asynchronous, clockmode, pulse mode with suitable examples. [8+8]
7. (a) Determine the equivalence classes for the given state - table.
- (b) Obtain final transition table. [8+8]

Present state q^v	Next state q^{v+1}, x^2				Output z^v			
	x=0	x=1	x=2	x=3	x=0	x=1	x=2	x=3
q_0	q_4	q_2	q_1	q_4	1	0	1	1
q_1	q_2	q_5	q_4	q_1	0	1	1	0
q_2	q_1	q_0	q_3	q_5	1	0	1	1
q_3	q_6	q_5	q_4	q_1	0	1	1	0
q_4	q_2	q_5	q_3	q_4	0	1	1	0
q_5	q_2	q_5	q_3	q_7	1	1	0	0
q_6	q_3	q_0	q_1	q_5	1	0	1	1
q_7	q_1	q_2	q_4	q_5	1	0	1	1

8. (a) Draw the ASM chart for the following state transistion, start from the initial state T_1 , then if $xy=00$ go to T_2 , if $xy=01$ go to T_3 , if $xy=10$ go to T_1 , other wise go to T_3 .
- (b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]

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1. Convert the following to Decimal and then to Octal.
 - (a) 4234_{16}
 - (b) $125F_{16}$
 - (c) 10010011_2
 - (d) 10111111_2
 - (e) 392_{10}
 - (f) 779_{10} [3+3+3+3+2+2]
2. (a) For the given Boolean function $F = xy'z + x'y'z + w'xy + wx'y + wxy$ [8]
 - i. Draw the logic diagram
 - ii. Simplify the function to minimal literals using Boolean algebra.
- (b) Obtain the Dual of the following Boolean expressions. [8]
 - i. $AB'C + AB'D + A'B'$
 - ii. $A'B'C + ABC' + A'B'C'D$
 - iii. $ABCD + ABC'D' + A'B'CD$
 - iv. $AB + ABC'$
3. (a) What do you mean by don't care combinations? [4]
- (b) What you mean by min terms and max terms of Boolean expressions. [4]
- (c) Simplify the Boolean function using K-map $F = \sum m(0, 1, 3, 4, 5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$ [8]
4. (a) A combinational circuit is defined by the following three functions $F_1 = \bar{x}\bar{y} + xy\bar{z}$ $F_2 = \bar{x} + y$ $F_3 = xy + \bar{x}\bar{y}$ Design the circuit with a decoder and external gates.
- (b) List the applications of Multiplexer and Demultiplexer. [12+4]
5. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

- (b) For the given 3-input, 4-output truth table of a combinations circuit, tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

6. (a) Find a modulo-6 gray code using k-Map & design the corresponding counter.
 (b) Compare synchronous & Asynchronous. [10+6]
7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output $Z = 1$ and overlapping is also allowed.
- (a) Obtain State - Diagram.
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 (b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]
