

III B.Tech II Semester Supplementary Examinations, Apr/May 2008
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. Implement the following logic functions using CMOS logic

(a) $Y = \{(A + B).C\}^1$

(b) $Y = \{(A.B + C).D\}^1$ [8+8]

2. Define an integrated circuit and explain clearly different Integrated Circuit design techniques using suitable examples. [16]
3. Design a stick diagram for two-input N-MOS NAND and NOR gates. [16]
4. Design a layout for CMOS 2-input NAND gate. [16]
5. (a) With respect to testability of a Digital design define controllability and observability .
- (b) Explain the properties of testable digital circuit. [8+8]
6. Draw the Architecture of PLA and explain how different logic functions can be implemented using PLA. [16]
7. How would you translate a register - transfer structure into a legal two - phase latched sequential machine? [16]
8. Explain about design methodology for 1BM ASICS. [16]

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1. Implement the following gates with n-MOS transistors only and explain its working
 - (a) 2 - Input NAND gate.
 - (b) 3 - Input NOR gate. [8+8]
2. Define different current parameters of Digital IC and explain their significance. [16]
3. Design a stick diagram for two-input N-MOS NAND and NOR gates. [16]
4. Compute the high-to-low delay of a two-input static complementary NOR gate with minimum-sized transistor driving these loads.
 - (a) An inverter with minimum-sized pull up and pull down.
 - (b) An inverter whose pull up and pull down are both of size $W = 10\lambda$ $L = 10\lambda$. [8+8]
5. Explain how wire delay are calculate using El-more - delay model and RC Trees. [16]
6. Draw the structure of a carry look ahead adder and explain its working principle. [16]
7. Explain clearly the detailed routing phase of the floor planning of the chip with few examples by considering all constraints. [16]
8. Sketch the architecture of the kitchen timer chip and explain about its architecture design. [16]

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1. Implement the following gates with n-MOS transistors only and explain its working
 - (a) 2 Input AND gate
 - (b) 4 Input NOR gate. [8+8]
2. Explain clearly about each step of typical design abstraction ladder for digital integrated circuits. [16]
3. What is a stick diagram and explain about different symbols used for components in stick diagram. [16]
4. Implement 3-input NOR gate and 2 input AND gates using static complementary logic. [16]
5. Give tests for stuck-open fault for each transistor in a two-input static NOR gate. [16]
6. Draw the structure of carry select adder and explain its working principle. [16]
7. How would you translate a register - transfer structure into a legal two - phase latched sequential machine? [16]
8. Draw the state transition graph for the kitchen timer chip's controller. [16]

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1. Implement the following gates with CMOS Logic and explain its working
 - (a) Ex-OR gate.
 - (b) 2 Input NOR gate. [8+8]
2. What are the key advantages of ICs? And explain how these advantages of ICs translate in to advantages at the system level. [16]
3. Explain with neat sketches CMOS fabrication using P - well process. [16]
4. Design a layout for CMOS 3-input NAND gate. [16]
5. Explain in detail the path - delay measurement of the combinational logic circuits. [16]
6. Draw the circuit diagram of four transistor DRAM cell with storage nodes and explain its working. [16]
7. Explain about the data - path controller architecture of register transfer machine. [16]
8. Explain about different types in the register file based data-path. [16]
