

IV B.Tech II Semester Regular Examinations, Apr/May 2008
VLSI DESIGN

(Electrical & Electronic Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in Saturation region.
(b) An nMOS transistor is operating in saturation region with the following parameters. $V_{GS} = 5V$; $V_{tn} = 1.2V$; $W/L = 110$; $\mu_n C_{ox} = 110 \mu A/V^2$. Find Transconductance of the device. [8+8]
2. With neat sketches explain how npn transistor is fabricated in Bipolar process. [16]
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A + B).C}$ [16]
4. Design a layout diagram for the PMOS logic shown below $Y = \overline{(A + B).C}$ [16]
5. Calculate on resistance of the circuit shown in Figure 5 from V_{DD} to GND. If n-channel sheet resistance $R_{sn} = 10^4 \Omega$ per square and p-channel sheet resistance $R_{sp} = 2.5 \times 10^4 \Omega$ per square. [16]

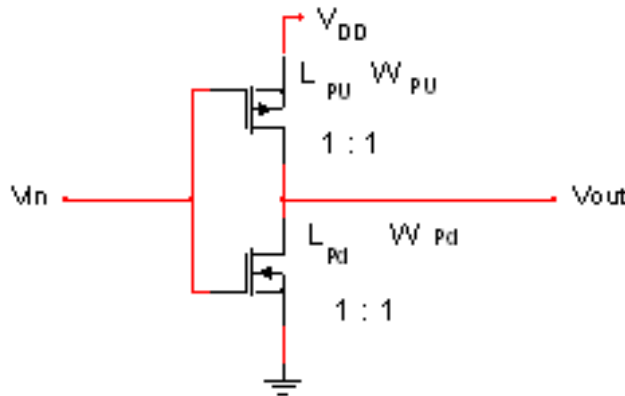


Figure 5

6. Using PLA Implement Half-adder circuit. [16]
7. What are the different report files that are provided by the place and route tool and discuss clearly about each report file. [16]
8. With neat sketches explain the oxidation process in the IC fabrication process. [16]

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1. (a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in linear region.
 (b) A PMOS transistor is operating in saturation region with the following parameters. $V_{GS} = -5V$; $V_{tp} = -1.2V$; $W/L = 95$; $\mu_n C_{ox} = 95 \mu A/V^2$
 Find Trans conductance of the device. [8+8]
2. With neat sketches explain how Diodes and Resistors are fabricated in nMOS process. [16]
3. Design a stick diagram for two input CMOS NAND and NOR gates. [16]
4. Design a layout diagram for CMOS inverter. [16]
5. Calculate ON resistance from V_{DD} to GND for the given inverter circuit shown in Figure 5, If n-channel sheet resistance is $3 \times 10^4 \Omega$ per square. [16]

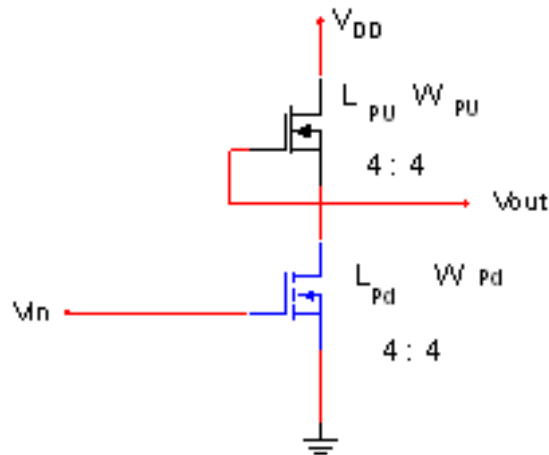


Figure 5

6. Clearly discuss about the following FPGA Technology
 - (a) Anti fuse Technology.
 - (b) Static RAM Technology. [8+8]
7. Explain about the following EDA tools.
 - (a) Design Rules verification.
 - (b) Layout vs Schematic verification.

(c) RC calculation from layout.

[5+6+5]

8. Mention different growth technologies of the thin oxides and explain about any one technique. [16]

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1. (a) Derive an equation for Transconductance of an n-channel enhancement MOSFET operating in Active region. Also write about figure of merit of MOSFET. [10+6]
- (b) For the arrangement shown below plot the on-resistance of M as a function of V_G . Assume $V_{tn} = 0.7$ V; $W/L = 10$; $\mu_n C_{ox} = 50 \mu\text{A}/\text{V}^2$
Note the drain terminal is open. (Figure 1b)

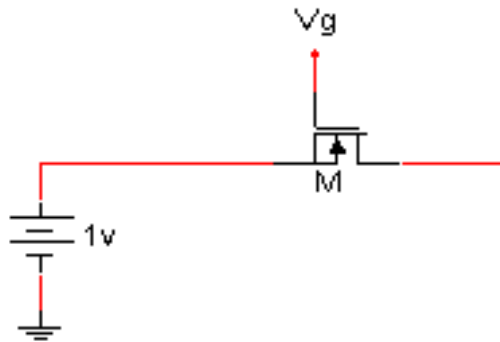


Figure 1b

2. (a) With neat sketches explain how resistors and capacitors are fabricated in p-well process.
- (b) With neat sketches explain how resistors and capacitors are fabricated in n-well process. [8+8]
3. Design a stick diagram for two input CMOS NAND and NOR gates. [16]
4. Design a layout diagram for CMOS inverter. [16]
5. Calculate ON resistance from V_{DD} to GND for the given inverter circuit shown in Figure 5. If n-channel sheet resistance is $2 \times 10^4 \Omega$ per square. [16]

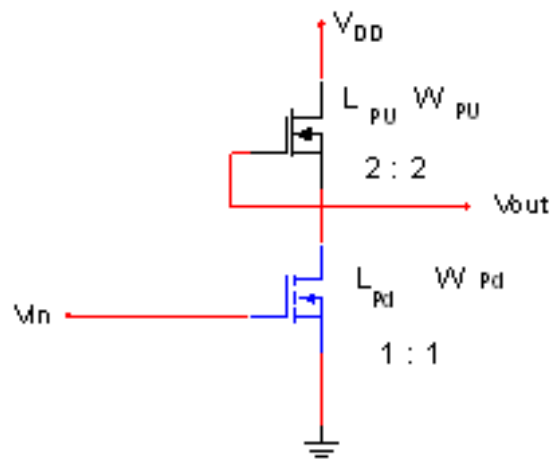


Figure 5

6. (a) What are the advantages and disadvantages of the reconfiguration.
 (b) Mention different advantages of Anti fuse Technology. [8+8]
7. Name different layout analysis and design tools? Explain the job of these tools. [16]
8. Mention different growth technologies of the thin oxides and explain about any one technique. [16]

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1. (a) With neat sketches explain the formation of the inversion layer in P-channel Enhancement MOSFET.
(b) An NMOS Transistor is operated in the triode region with the following parameters $V_{GS} = 4V$; $V_{tn} = 1V$; $V_{DS} = 2V$; $W/L = 100$; $\mu_n C_{ox} = 90 \mu A/V^2$
Find its drain current and drain source resistance. [8+8]
2. With neat sketches explain how Diodes and Resistors are fabricated in Bipolar process. [16]
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A + B + C)}$ [16]
4. Design a layout diagram for the CMOS logic shown below $Y = \overline{(A + B + C)}$ [16]
5. Calculate the gate capacitance value of $2\mu m$ technology minimum size transistor with gate to channel capacitance value is $8 \times 10^{-4} pF/\mu m^2$. [16]
6. Using PLA Implement JK Flip flop circuit. [16]
7. With respect to synthesis process explain the following terms.
(a) Flattening
(b) Factoring.
(c) Mapping. [6+5+5]
8. With neat sketches explain the ION- lithography process. [16]
