

Code No. 21/VLSI

OR

**JAWAHARLAL NEHRU TECHNOLOGY UNIVERSITY, HYDERABAD
M .Tech. II Semester Supplementary Examinations, March – 2009
PHYSICAL DESIGN AUTOMATION
(VLSI System Design)**

Time: 3 hours

Max. Marks.60

**Answer any Five questions
All questions carry equal marks**

- 1.a) Explain about the three design domains in VLSI.
b) Give the visualization of the three design domains in gajskis y-chart, with explanation.
- 2.a) In what situations, layout compaction can be applied? Explain.
b) Explain about Liao-wong Algorithm. Compare the same with the bell man-ford Algorithm.
c) How placement Algorithms are grouped? What are the different approaches for perturbation of a feasible solution for standard cell? Explain.
- 3.a) Assume a particular digital circuit and give its structural description and floor plan for the same.
b) Sketch a floor plan with labeled horizontal and vertical line segments. Draw its polar horizontal graph and polar vertical graph giving explanation.
- 4.a) Explain about area routing problems.
b) Describe the 'Classical model' used for channel routing.
5. What is left edge algorithm? How it helps in finding solution to routing problems? Explain about Global routing.
- 6.a) Explain about important abstraction levels for which specific simulation tools are developed.
b) Compare gate modeling and delay modeling.
- 7.a) Explain how ROBDD manipulation is done.
b) Describe how ROBDD can be used to logic verification.
8. Write notes on any two:
 - a) Conditional data flow
 - b) Mobility-based scheduling
 - c) High level Transformations.
